UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,707	05/11/2001	Liwei Chour	3626-0197P	5178

2292 7590 11/12/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
BRODA, SAMUEL	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,707	CHOUR, LIWEI	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

Drawings

2. Applicant's formal drawings have been reviewed and approved by the PTO Draftsperson.

Claim Rejections - 35 U.S.C. § 112, First Paragraph

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3.1 Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

3.2 Regarding independent claim 6, this claim reads as follows:

A computer-aided layout design method, comprising:

displaying a layout image of at least a portion of a layout;

detecting at least one defect of the layout; and

generating an enlarged image of the defect, and displaying the enlarged image simultaneously with the layout image.

However, the Specification fails to provide any description regarding:

(1) how a layout defect is identified;

(2) how the layout defect, once identified, is correlated with a portion of the layout image; and

(3) how the portion of layout image containing the defect is enlarged and viewed.

Additionally, the Specification appears to lack flowcharts or other text describing the steps necessary to perform the method of claim 6. See MPEP Section 2106.02; see especially column 1 page 2100-27 (Rev. 2, May 2004).

The Specification and accompanying figures do not appear to teach how one could make and/or use the invention but instead appear to describe the benefits of such an invention. Taken as a whole, only with undue experimentation could one reasonably skilled in the art make and/or use the invention, because of the omissions in the subject matter described in the Specification.

3.3 Claims 7-10 are each dependent on independent claim 6 and is rejected using the same analysis.

3.4 Claims 1-5 are the corresponding system claims of method claims 6-10 and are rejected using the same analysis. Although the Specification refers to a "defect-detecting module 11," a "zoom-lens module 12," and an "information-display module 13," the Specification appears to contain no information regarding how these modules are: (1) individually programmed to operate; and (2) connected to work together.

Claim Rejections - 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> . . .
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.1 Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Anonymous, "Visual Fault Analyzer (VFA TM) Speeds PCB Fault Diagnostics and Repair," webpage available at: http://www.intellitech.com/company/PCB_fault_diagnostics_repair.asp (February 2000)(the "Web Page").

4.2 Regarding claim 6, Anonymous teaches a computer-aided layout design method, comprising:

displaying a layout image of at least a portion of a layout [layout displayed in upper right sub-window of Visual Fault Analyzer, Web Page at 1];

detecting at least one defect of the layout ["Stuck at 0" defect detected, right sub-windows of Visual Fault Analyzer, Web Page at 1]; and

generating an enlarged image of the defect, and displaying the enlarged image simultaneously with the layout image ["Image of Device Under Test with Faults Overlayed" displayed in main left sub-window of Visual Fault Analyzer, Web Page 1].

Therefore, Anonymous anticipates claim 6.

4.3 Regarding claim 7, the Visual Fault Analyzer permits the user to "Toggle the VFA view to display the backside of the PCB, or to select layers within a layout database." Web Page at 3 paragraph 1.

4.4 Regarding claims 8-9, the Visual Fault Analyzer "[a]llows user to select which failures to display, from a single net fault to all failures. Selections can be made using the fault type and/or net name." Web Page at 3 paragraph 1. Therefore the Visual Fault Analyzer automatically performs enlarge ratio adjustments based on user input, and permits switching between the types of failures to display.

4.5 Regarding claim 10, the Visual Fault Analyzer displays fault detail information in the right-bottom sub-window. Web Page at 1.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to McKay et al, U. S. Patent 6,418,551 is cited as teaching a design rules checking tool using a 'layout versus schematic' comparison.

Reference to Smith et al, U. S. Patent 6,185,707 is cited as teaching a an IC test software system for mapping logical functional test data to a physical representation.

Reference to Chevallier et al, U. S. Patent 6,115,546 is cited as teaching a method for managing data obtained during 'design rule check' and 'layout versus schematic' verification procedures.

Reference to Wu, U. S. Patent 5,781,446 is cited as teaching a method for multi-constraint domain electronic system design mapping.

Reference to Wagner, "Close Inspection," Machine Design, Vol. 72 No. 13, pp. S36 et seq (July 2000), is cited as teaching a frame-grabber image capture board.

Reference to Anonymous, "Visual Fault Analyzer --VFA-- Speeds PCB Fault Diagnostics and Repair; Easy-to-Use Fault Viewer Finds Hidden Faults and Lowers PCB Re-Work Costs," Business Wire (February 2000), is cited as disclosing a second press-release describing the "Visual Fault Analyzer."

Reference to Song et al, "S/390 G5 CMOS Microprocessor Diagnostics," IBM Journal of Research and Development, Vol. 43 No. 5/6, pp. 899-914 (September 1999), is cited as teaching the display of circuit layouts with the corresponding defects. See Figs. 7 and 9.

Reference to Lloyd et al, "Electromigration Wreaks Havoc on IC Design," EDN Vol. 43 No. 7, pp. 145-148 (March 1998), is cited as teaching the display of EM violations on a power grid. See Figs. 1 and 2 and corresponding text.

6. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (571) 272-3709. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska can be reached at (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER